Improved first generation current conveyor based on self-cascode current mirror

Beniamin Drăgoi, *Member, IEEE*

***Abstract* — This paper presents an improved first generation current conveyor. The proposed circuit is based on a CMOS translinear loop and self-cascode current mirrors. The structure of the circuit is analyzed and compared with a classical CCI structure. PSpice simulation results for the proposed circuit in 0.35µm CMOS technology are given to verify the theoretical analysis.**

***Keywords* — current conveyor, self-cascode mirror, CMOS.**

I. Introduction

SINCE Sedra published first generation current conveyor (CCI) (1968), current conveyor based circuits have received lots of attention in analog signal processing applications, such as filter [1] function generator [2], impedance function synthesis [3], etc. [4]. CCs are unity-gain amplifiers widely used by analog designers, in particular because they offer a number of advantages, such as better linearity, wider bandwidth, and design flexibility over conventional voltage-mode active devices.

Several types of CC exist covering first, second (CCII) and third generation (CCIII). Whilst CCII is considered the most versatile and used CC, the first generation CCI is well known for its simplicity.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

$$\begin{cases} I_Y = \pm I_z = I_x \\ V_x = V_Y \end{cases} \quad (2)$$

The definition matrix (1) along with input-output equations (2) and nodes impedance level (Table 1) presents the main characteristics of the ideal CCI (CCI+ and CCI-).

TABLE 1: CCI IMPEDANCE LEVELS

Node (CCI)	Impedance Level
X	0
Y	∞
Z	∞

The CCI symbol and CMOS structure are given in Fig. 1 and Fig. 2.

A good CCI structure must provide several features: very low X input impedance, very high Y and Z impedances, unity voltage and current gains between ports, large dynamic input and output current and voltage ranges.

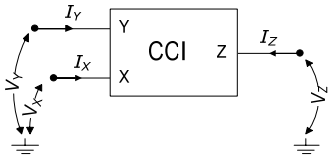

Fig. 1. CCI symbol

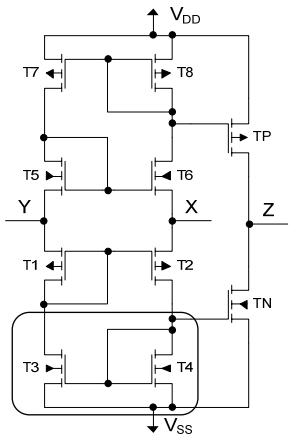

Fig. 2. Typical CMOS CCI+ structure

II. IMPROVED SELF-CASCODE CCI

A. Simple current mirror based CCI structure

The typical CMOS structure (Fig.2) is a class AB current conveyor that offers the advantages of high dynamic range, wide bandwidth and non-slew rate limited performance. Due to the low quality of the simple current mirror (CM) this CCI structure assures moderate performances in respect of input/output impedance.

Equations for input and output resistances for CCI in Fig.2 are given in (3), (4) and (5).

$$R_X \cong \left(\frac{g_{ds2} + g_{ds4}}{g_{m2} g_{m4}} + \frac{g_{ds1} + g_{ds3}}{g_{m1} g_{m2}} \right) \| \left(\frac{g_{ds5} + g_{ds7}}{g_{m5} g_{m6}} + \frac{g_{ds6} + g_{ds8}}{g_{m6} g_{m8}} \right) \quad (3)$$

$$R_Y \cong r_{o3} \| r_{o7} \quad (4)$$

$$R_Z \cong r_{oN} \| r_{oP} \quad (5)$$

To decrease the input resistance on port *X*, R_X, and increase input resistance on port *Y*, R_Y, and output resistance on port *Z*, R_Z, the designer must increase the CMs output resistance. An efficiently improvement cannot

Beniamin Drăgoi is with the Faculty of Electronics and Telecommunications, University Politehnica of Timisoara, Bul. V. Parvan nr. 2, 300223, Timişoara, Romania, (phone: +40745459956; e mail: beniamin.dragoi@etc.upt.ro).

be obtained due to CMs structure. This limitation imposes to replace simple CM with better current mirrors.

B. Cascode mirror based CCI structure

Several papers present AB class current conveyors using improved current mirrors: cascode mirror [5], high-swing mirror [6], low voltage self-cascode [7], etc. Fig. 3 shows a CCI based on cascode current mirror (CCM).

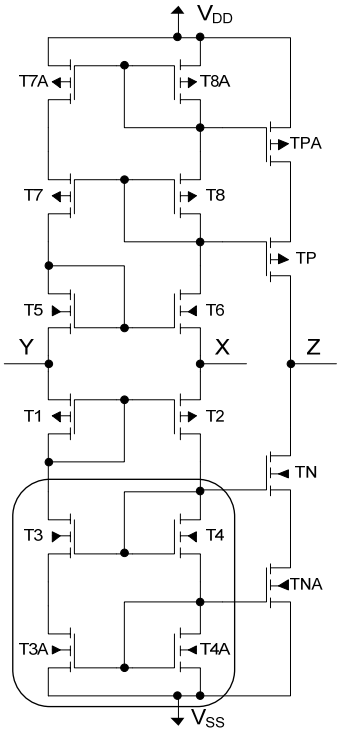

Fig. 3. Cascode mirror based CCI structure

This current mirror structure provides much greater output resistance (6) and thus CCI input and output resistances are improved.

$$r_o = r_{o3A}(g_{m3}r_{o3}) \tag{6}$$

CCM requires minimum input (7) and output voltage (8) larger than CM to keep all transistors in saturation.

$$V_{output,\min} = V_{th3} + 2*V_{DSsat} \tag{7}$$

$$V_{input,\min} = 2*(V_{th3A} + V_{DSsat3A}) \tag{8}$$

Using CCMs instead of CMs in CCI dramatically reduce input and output voltage dynamic ranges. This is a disadvantage than cannot be accepted for circuits that use low voltage power supply.

Replacing CCM with high-swing current mirror is out of purpose of this paper because requires additional bias circuitry that increases CCI complexity.

C. Self cascode mirror based CCI structure

The purpose of this paper is to propose and analyze a new AB class CCI structure based on self-cascode mirrors (SCCM). The proposed circuit is given in Fig. 4 and based on 6 SCCMs [8]. This structure maintains CCI circuit complexity as low as possible but provides good performance in terms of input and output resistances and voltage dynamic range.

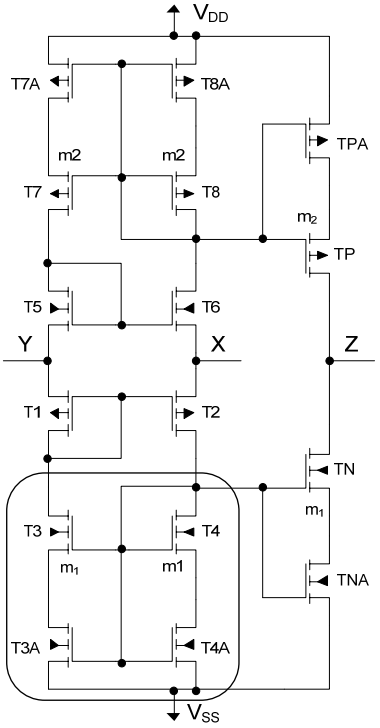

Fig. 4. New self-cascode CCI+

A well-designed SCCM must assure that all transistors work in saturation. Reference [8] shows a condition (9) to keep transistors *T3A* and *T4A* in saturation. This is easy to fulfill in a multi-threshold CMOS process.

$$V_{th4A} - V_{th4} \geq V_{DSsat4} \tag{9}$$

In a standard CMOS technology this condition can be accomplish using SCE (short-channel effect) and (10) [9].

$$\frac{\beta_{4A}}{\beta_4} \leq \left(\frac{n-1}{n} + \frac{V_{th4A} - V_{th4}}{V_{GS4A} - V_{th4A}} \right)^2 \tag{10}$$

n – slope factor (about 1.3), $\beta = \mu \cdot Cox \cdot W/L$.

Reference [10] presents a methodology based on SCE and RSCE (reverse short-channel effect) [11] useful to design both pMOS and nMOS SCCMs.

This kind of current mirror shows an output resistance similar to that of the cascode mirror but input and output voltage close to the simple CM. Table 2 gives a comparative view for output impedance, input and output voltage for the three current mirrors previous presented. It is obvious that SCCM is better than CM and equal with CCM regarding output resistance. SCCM demands a minimum input voltage similar with CM but much less than CCM. Minimum output voltage required by SCCM is less that similar voltage for CCM and very close to CM once. This SCCM shows improved output resistance without affecting voltage dynamic ranges.

Input and output resistances for CCI in Fig. 4:

$$R_X \cong \left(\frac{g_{ds2}g_{m4} + g_{ds4}g_{ds4A}}{g_{m2}g_{m4}g_{m4A}} + \frac{g_{ds1}g_{m3} + g_{ds3}g_{ds3A}}{g_{m1}g_{m2}g_{m3}} \right) \| \| \left(\frac{g_{ds5}g_{m7} + g_{ds7}g_{ds7A}}{g_{m5}g_{m6}g_{m7}} + \frac{g_{ds6}g_{m8} + g_{ds8}g_{ds8A}}{g_{m6}g_{m8}g_{m8A}} \right) \tag{11}$$

TABLE 2: CM, CCM AND SCCM MAINLY CHARACTERISTICS

	Current mirror CM	Cascode current mirror CCM	Self cascade current mirror SCCM
Output resistance	$r_o = r_{o3}$	$r_o = r_{o3A}(g_{m3}r_{o3})$	$r_o = r_{o3A}(g_{m3}r_{o3})$
Minimum output voltage	$V_{DSsat3A}$	$V_{th3} + 2*V_{DSsat}$	$V_{th3} - V_{th3A} + V_{DSsat}$
Minimum input voltage	$V_{th3} + V_{DSsat3}$	$2*(V_{th3A} + V_{DSsat3A})$	$V_{th4A} + V_{DSsat4A}$

$$R_Y \cong \frac{g_{m3}}{g_{ds3}g_{ds3A}} \| \frac{g_{m7}}{g_{ds7}g_{ds7A}} \quad (12)$$

$$R_Z \cong g_{mN}r_{oN}r_{oNA} \| g_{mP}r_{oP}r_{oPA} \quad (13)$$

Equations (11), (12) and (13) show that new CCI structure achieves greater resistances on ports *Y* and *Z* and smaller resistance on port *X*.

Fig. 5 shows CCI- structure based on self cascade current mirror.

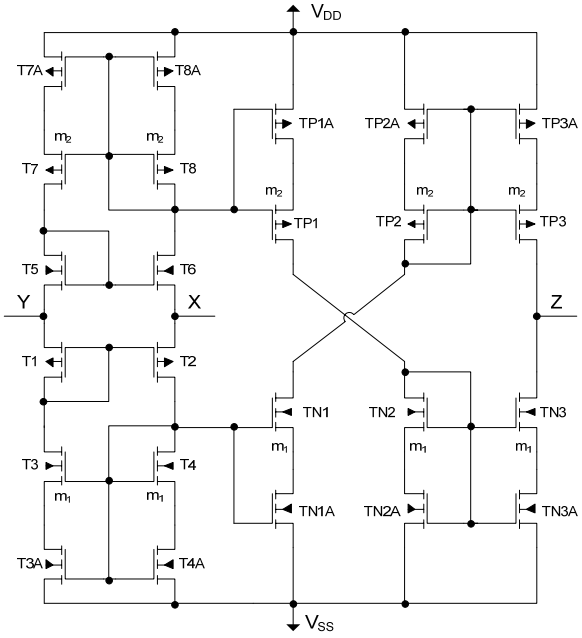

Fig. 5. Self-cascode CCI-

III. DESIGN CIRCUITS

Both circuits from Fig. 2 and Fig. 4 were designed in a standard 0.35µm CMOS technology. All the transistors in Fig. 4 were designed to work in saturation mode using (10) and SCE for sizing nMOS and RSCE for sizing pMOS [10]. Table 3 and Table 4 show W and L sizes for transistors in Fig. 2 and Fig. 4.

TABLE 3: W AND L SIZES FOR SELF-CASCODE CCI+

CCI+ new	*W*[µm]	*L*[µm]
T_1, T_2	26	3.3
T_3, T_4, T_N	68.4	1
T_{3A}, T_{4A}, T_{NA}	3.8	0.65
T_5, T_6	10.2	2.8
T_7, T_8, T_P	96	0.55
T_{7A}, T_{8A}, T_{PA}	32	3.4

TABLE 4: W AND L SIZES FOR TYPICAL CCI+

CCI+ typical	*W*[µm]	*L*[µm]
all nMOS	15	2.5
all pMOS	55.5	2.5

IV. SIMULATION RESULTS

The circuit was simulated using PSpice. Using power supplies of ±2.5V and the sizes in Table 3 and Table 4 self-bias currents are 110µA for Fig. 2 and 55µA for Fig.4. Table 5 shows the input and output impedances, voltage and current gains, bias currents and active areas for the proposed CCI+ and for a typical CCI+. For almost the same active area the new CCI provides the same input resistance on port X but the bias current is halved. There are good improvements in respect of input impedance on port *Y* – 13.5 times and output impedance on port *Z* – 8 times. Current gains β and γ errors are reduced from 0.7% to 0.11%. Voltage gain α is reduced from 0.72% to 0.38%.

TABLE 5: NEW CCI+ VERSUS TYPICAL CCI+ PERFORMANCES

	CCI+ new	*CCI+ Typical*	
Technology	CMOS 0.35µm, ±2.5V		
Active area	926	881	μm^2
Bias current	55	110	µA
Rx	20.02	19.12	Ω
Ry	6.86	0.507	MΩ
Rz	10.89	1.36	MΩ
V_X/V_Y (α)	0.9962	0.9928	
I_Z/I_X (β)	1.0011	1.007	
I_Y/I_X (γ)	0.9989	0.993	
Cy	105	130	fF
Cz	85	55	fF

Fig. 6 shows input and output impedances for both the new CCI+ and a typical CCI+.

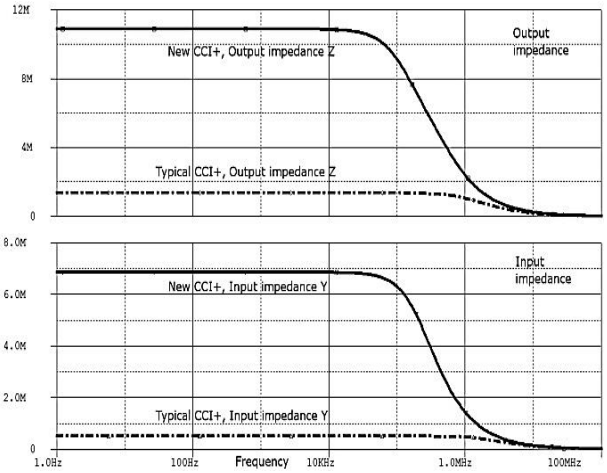

Fig. 6. Input/output impedances for new and typical CCI+

Fig. 7 presents the voltage tracking error between *Y* and *X* ports. It can be seen that the input voltage range is almost the same for the new CCI based on SCCM as for the typical CCI based on CM.

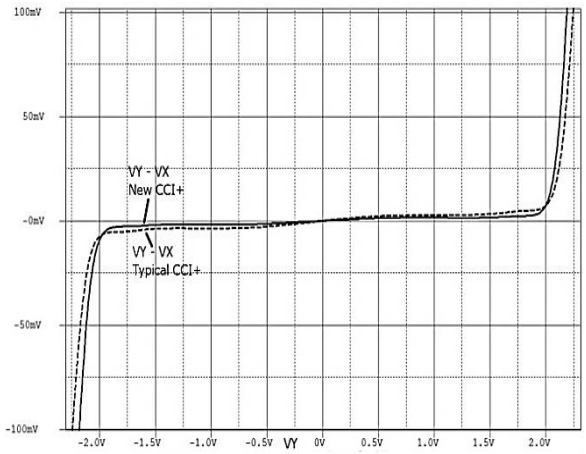

Fig. 7. Input voltage tracking error between ports *Y* and *X*

To demonstrate the usefulness of the improved features for the CCI next are presented two applications for this circuit – negative impedance convertor (NIC) and negative admittance/impedance convertor (NAIC). Fig. 8 and Fig. 9 show these circuits.

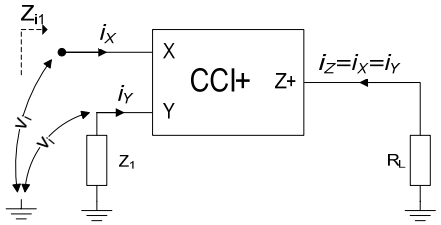

Fig. 8. NIC based on CCI+

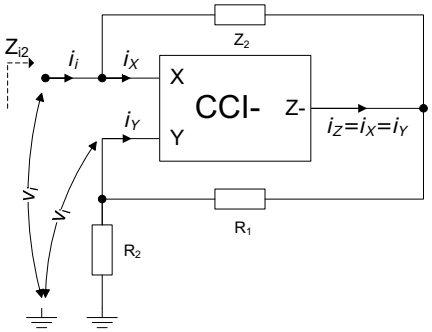

Fig. 9. NAIC based on CCI-

NIC input impedance is given by (14) and NAIC input impedance is given by (15)

$$Z_{i1} = \frac{v_i}{i_X} = \frac{v_i}{i_Y} = -Z_1 \tag{14}$$

$$Z_{i2} = \frac{v_i}{i_i} = -\frac{1}{Z_2} R_1 R_2 = -Y_2 R_1 R_2 \tag{15}$$

Both circuits were simulated with typical CCI and new CCI. Fig. 10 shows simulation results. Z_1 and Z_2 are capacitors with value 10pF and resistors have equal values, $R_1=R_2=100k\Omega$. For circuits designed using CCI based on SCCM input impedances have extended frequency ranges where close approximate an ideal behavior. Frequency ranges are extended with more than 1.5 decades towards lower frequency. This improvement is consequence of higher input and output resistance on ports *Y* and *Z* for new first generation current conveyor.

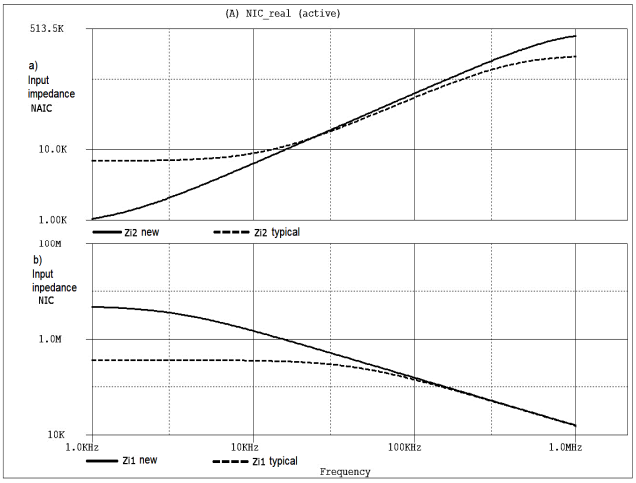

Fig. 10. a) NAIC input impedance and b) NIC input impedance for both new and typical CCI

V. CONCLUSION

This paper has presented a novel CCI structure based on self-cascode current mirror. The results show that the proposed circuit improves performances in respect of input/output impedances and voltage/current gains maintaining large dynamic voltage ranges.

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