A Low-Power and High Gain CMOS UWB Power Amplifier for Group 1~3 MB-OFDM Application

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***Abstract* —The design of a 3−8 GHz UWB CMOS power amplifier (PA) for group 1~3 MB-OFDM applications in UMC 0.13µm CMOS technology is presented in this work. To obtain high gain and low power consumption PA is composed of two stages including cascode topology with an additional common-source stage used for the second stage. To achieve sufficient linearity and efficiency both stages operate in the Class-AB regime. The LC based networks are used to provide good input and output impedance matching. The resistive feedback is utilized in both stages to enhance bandwidth and improve wideband matching. Simulation results indicated that the input return loss (S_{11}) was less than −6 dB, the output return loss (S_{22}) was less than −3 dB, and reverse isolation (S_{12}) was less than −41 dB over frequency range of interest. Maximal gain (S_{21}) was 17.1 dB at 5.5 GHz while average gain was approximately 15 dB. Output 1-dB compression was 0.8 dBm. The PA presented offers excellent PAE of 15.3% with very low power consumption of 11.2 mW at 1.2 V.**

***Keywords* — Cascode topology, CMOS integrated circuits, MB-OFDM ultra-wideband power amplifier, RF transmitters.**

I. Introduction

ULTRA-WIDEBAND (UWB) communication by means of short "carrier-free" pulses was first conceived in "time-domain electromagnetics" in the 1960s, when it was only used in military and radar applications [1]. Today, wireless technology is becoming one of the most promising for both academic and industrial circles due to the wide spectrum of frequency bands for very high data rate up to 480 Mb/s with very low power over short range. Recently, UWB standard is highly used in short range wireless sensor networks, the position detection systems, tumor detection system and many other medical applications. FCC (Federal Communications Commission) defines a signal as ultra wideband if it occupies 500 MHz of radio frequency spectrum or exhibits a fractional bandwidth of 25% [2]. Since the FCC allocated the frequency spectrum for UWB technology is 3.1−10.6 GHz, the power level from the UWB transmitter should be small enough not to interfere with the already existing communication systems such as WLAN, Bluetooth and GSM. This requirement limits output power level of UWB TXs at −41.25 dBm/MHz [2]. To satisfy all the constraints UWB transceivers require the usage of wideband, low power and low cost circuits which further complicates design of RF front end blocks like power amplifier (PA), low noise amplifier (LNA), and mixer. Nowadays, the RF circuits are mostly realized in CMOS technology due to its advantages of low price, small size, high integration, and low power consumption.

There are several proposals for realization of short range high data rate UWB standard. In this work MultiBand Orthogonal Frequency Division Multiplexing (MB-OFDM), proposed by WiMedia [3], has been used. MBOA (MultiBand OFDMA Alliance) was divided the frequency range from 3.168 GHz to 10.560 GHz into 14 bands. Each band consists of 128 subchannels, has bandwidth of 528 MHz with central frequency given by m×264 MHz, for odd values of m from 13 to 39. All 14 channels are divided into five groups, where each group consists of three channels and the last group is composed of only two channels. The first three groups from 3.168 GHz to 7.92 GHz are denoted as Group 1, Group 2 and Group 3 as shown in Fig. 1.

A broadband CMOS power amplifier which can operate in the frequency range of 3 GHz to 8 GHz for group 1~3 MB-OFDM UWB applications is described in this paper.

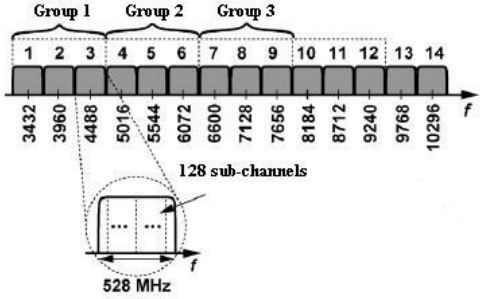

Fig. 1 MBOA band structure and channelization.

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Since the output power level of UWB signals must be too low to match the power mask of FCC (to prevent interference with the already existing communication systems), the proposed design only focused on gain, bandwidth, linearity, efficiency and power consumption of the UWB PA. The single-ended topology is employed because most existing components designed to be driven by PAs are single-ended. LC filter method is utilized to obtain good impedance matching. To increase power gain without additional power consumption a cascode topology is used for the second PA stage. The first PA stage is the common source amplifier combining with the inductive source degeneration to achieve the wideband input matching. The resistive feedback is used in both PA stages to realize the wideband specifications.

Section II describes wideband impedance matching techniques and some of the designed circuit details. Simulation results are given in Section III, while the conclusions are discussed in Section IV.

II. WIDEBAND MATCHING TECHNIQUES

There are several types of wideband amplifier topologies: the distributed amplifiers, the resistive shunt feedback amplifiers and the bandpass filter-based input matching amplifiers.

The distributed amplifiers are quite common for broadband circuit realizations [4]. Though good linearity and matching can be achieved over a wideband of frequencies, the power consumption and area occupied by these circuits can be quite high due to the multiple amplifying stages.

Another common topology for wideband amplifiers is the shunt feedback amplifiers usually comprising a resistor (Fig. 2).

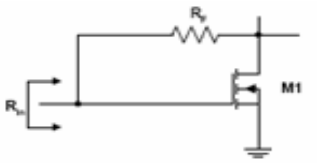


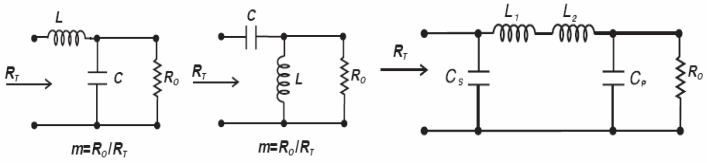
Fig. 2 Resistive shunt feedback for broadband matching.

This method can provide good wideband matching at both input and output ends, and has the extra advantages of providing circuit stability and in achieving the flat gain response. For a transistor stage with gain A_v, the input resistance can be calculated as:

$$R_{in} = \frac{R_F}{1 + A_v}. \quad (1)$$

The value of the feedback resistance R_F has to be selected according to the matching and gain requirements of the amplifier. A small R_F can provide excellent matching but the gain of the amplifier drops due to significant signal feedback through this path. On the other hand, a large R_F can provide good gain but reduces the effect of feedback. Through careful simulations, the optimum value of R_F can be achieved for the best matching and gain conditions. Disadvantage of this topology is requirement of rather large amount of current in the CMOS process due to the strong dependence for voltage gain on the transconductance of the amplifying transistor. In many cases in literature instead of this topology, a shunt feedback composed of capacitor and resistor in series can be found. The capacitor is added to prevent the DC current from flowing directly through the shunt feedback path to the output terminal.

Typical narrowband applications use LC based networks to achieve matching at a particular frequency by exploiting the fact that the impedance of the network is resistive at the resonant frequency. Using filter theory, this approach can be extended for wideband matching conditions. The most common impedance matching networks used in RF PA design are shown in Fig. 3 [5].



a) b) c)

Fig. 3 Basic RF matching networks: a) Low-pass network, b) High-pass network, and c) π-network.

Main advantage of this matching topology is its simple realization. However, multiple LC stages might be needed in some cases for broadband matching and they can occupy a substantial die area. This could cause problems in die-limited implementation.

III. ULTRA-WIDEBAND PA DESIGN

The proposed two stages UWB PA design is shown in Fig.4. To provide the bandwidth requirement and the high power gain with low power consumption, both the cascade and cascode topology have been used. Increase in the gain and gain flatness can be obtain by cascade topology, while usage of cascode topology can reduce some parasitic capacitance effects which degrade the gain performance at high frequency, and achieve higher gain for the same power consumption. As MB OFDM application also requires good efficiency and linearity both stages operate in Class-AB regime. To obtain good impedance matching LC networks are used at the input (inductor L_{in} and capacitor C_{in}) and at the output (inductor L_{out} and capacitor C_{out}) of the PA. The inductor L_1 and L_3 values are chosen large enough to provide high impedance path to RF signal

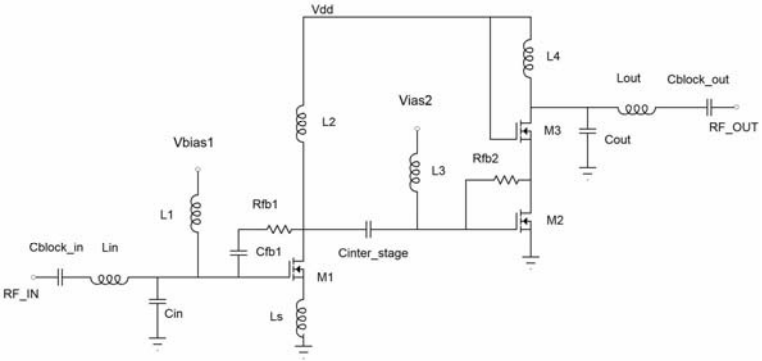


Fig. 4 The designed 3−8 GHz CMOS UWB PA.

and to stop its flowing to bias circuit. The first stage is CS inductive degenerated amplifier modified with the shunt feedback of resistor R_{fb1} and capacitor C_{fb1} to enhance bandwidth and improve wider input matching. The capacitor C_{fb1} is used to prevent the DC current from flowing directly through the shunt feedback path to the output terminal. V_{bias1} and V_{bias2} represent polarization signals for the first and the second stages, respectively. Bias circuit consists of two current mirrors which have one common branch to save area. $C_{block\text{-}in}$ and $C_{block\text{-}out}$ are input and output DC blocking capacitors. Inductor L_2 is a load for CS amplifier M_1.

The first and second stages are connected with interstage capacitor C_{block}. The second stage consists of cascode amplifier (composed of M_2 and M_3 transistors) with resistive feedback (resistor R_{fb2}) to obtain flat gain and enhance output matching. As additional shunt feedback capacitor was caused decrease in gain bandwidth, it is not used in this amplifying stage. Inductor L_4 is a load of cascode topology.

IV. Simulation Results

The designed UWB PA has been simulated using SpectreRF Simulator from Cadence Design System in standard UMC 0.13µm CMOS eight-metal technology. Supply voltage of this technology is 1.2 V. As wideband PA has been designed for frequency range from 3 GHz to 8 GHz, input source at 5 GHz frequency has been used. PA topology was optimized with the main aim to improve voltage gain and minimize power consumption while still keeping acceptable values for remaining Figures of Merits (FOMs). The simulation results for the input (S_{11}) and output (S_{22}) return loss, small signal gain (S_{21}) and reverse isolation (S_{12}) are shown in Figs. 5 and 6. These parameter values are obtained using S-parameter analysis. As could be noticed, the gain performance of this UWB PA is presented by S_{21} parameter. The maximum gain is 17.1 dB at 5.5 GHz, while the average gain is obtained about 15 dB from 3 GHz to 8 GHz. The achieved input (S_{11}) and output (S_{22}) return loss are less than −6 dB and −3 dB, respectively, over the frequency range of interest. S_{11} minimal value was −31.44 dB at 4.59 GHz, whereas S_{22} minimal value was −27.22 dB at 7.49 GHz. S_{22} values less then −3 dB at lower frequencies could be obtained if S_{22} minimal value was shifted at the lower frequency. This change would cause decrease in gain bandwidth and gain values at higher frequency. Parameter S_{12} represents the reversed transmission (voltage gain) or reversed isolation. Its value must be less than −20 dB to have good isolation between PA output and input [5-7]. In this paper, reverse isolation less than −41 dB across the whole required band is achieved. Alternate stability factors are K_f and B_{1f}. The unconditional stability requirements of an circuits are K_f >1 and B_{1f} >0. In this work, K_f is higher than 7.8 and B_{1f} is higher than 0.5 over the frequency range of interest.

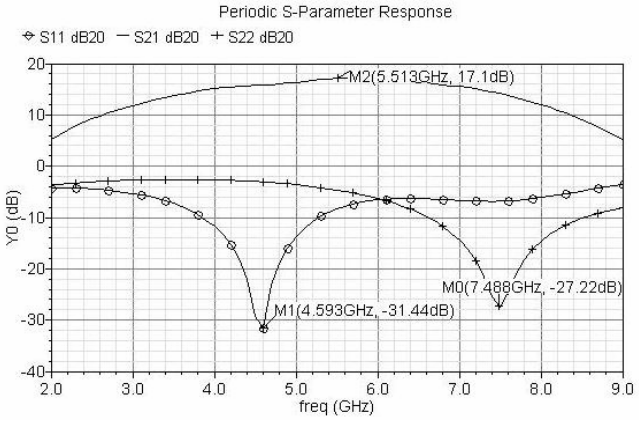


Fig. 5 Simulation results for the input and the output return loss, and small signal gain.

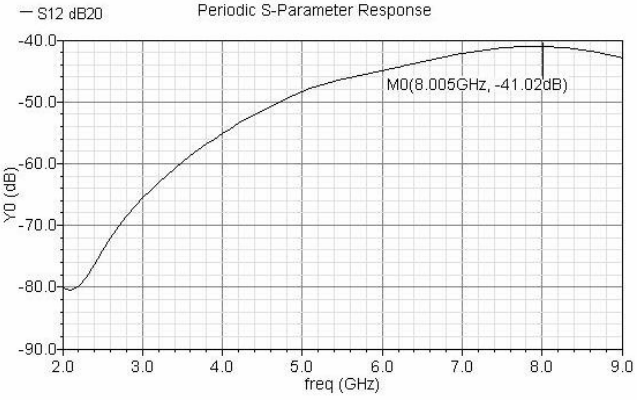


Fig. 6 Simulation results for the reverse isolation.

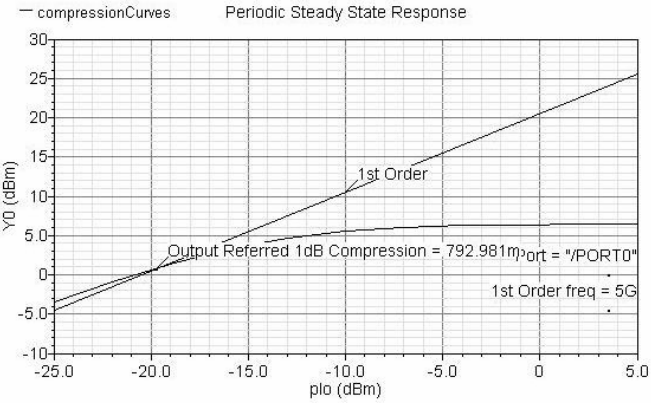


Fig. 7 Simulated 1-dB compression point at output ($OP_{1\text{-}dB}$).

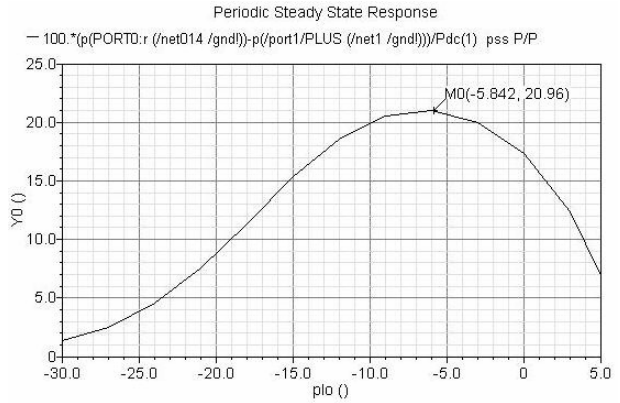


Fig. 8 Simulated input power vs. PAE (Power Added Efficiency).

Although the gain is a major PA Figure of Merit, the linearity is quite important as well. This parameter limits the actual power that can be driven to the load by the PA. The power amplifier can drive the wanted signal without too much harmonic terms only if operates in the linear region. Two typical linearity merits are output 1-dB compression point (OP_{1dB}) and the input (IIP3) or the output (OIP3) third order intercept point, which represent the nonlinear gain compression and intermodulation effects, respectively [6, 7]. To simulate IP3 parameter in Cadence Design System, Periodic Steady State (PSS) analysis with two large signals at 5 GHz and 5.1 GHz has to be used. As this analysis can cause convergence problem in simulator, for linearity merit only 1-dB compression point is used in this work.

Relation between these two linearity parameters is given by:

$$IP3 \approx P_{1\text{-}dB} + 10 \text{ dBm}. \quad (2)$$

The output 1-dB compression point is 0.8 dBm as shown in Fig. 7. Total power consumption (P_C) is 11.2 mW, where PA power consumption is 9.72 mW and P_C of bias circuit is 1.48 mW.

Finally, Fig. 8 shows the simulated power added efficiency (PAE) vs. input power (*plo*). As it can be seen from the simulation results, the maximum PAE of 20.96% could be obtain for input power of −5.84 dBm (at 5 GHz). For presented PA performance PAE was around 15.3%.

The comparisons of the obtained PA Figures of Merit with values found in literature [8−11] are summarized in Table I. As PA for MB-OFDM UWB applications designed in 0.13 μm CMOS technology could not be found in literature, achieved features were compared with PAs designed in 0.18 μm CMOS technology. Reference [8] had achieved high linearity and good input and output matching, but with small PAE and very high power consumption. In [9] good PAE had obtained but with quite low gain. The design proposed in [10] has very poor PAE. Reference [10] has higer power consumption and lower gain and PAE in comparison to presented PA topology. As it can be seen, proposed PA design in this work has been obtained higher gain and PAE with considerably lower power consumption compared to values found in published papers. Other PA Figures of Merits are comparable to values given by other authors [8−11].

TABLE 1: SUMMARY OF SIMULATION RESULTS AND COMPARISON OF UWB PA PERFORMANCES.

Ref.	[8]	[9]	[10]	[11]	This work
Tech. (μm)	0.18	0.18	0.18	0.18	0.13
Supply Volt. (V)	2	1.5	1.8	1.8	1.2
Freq. (GHz)	3−10	6−10	3.1−10.6	3.0−7.5	3−8
S_{11} (dB)	<−10	<−7	<−6	<−5	<−6
S_{22} (dB)	<−10	<−3	<−8	<−7	<−3
Aver. Gain (dB)	11	8.5	9	10	15
$OP_{1\text{-}dB}$ (dBm)	8	5	>0	>0	0.8
PAE (%)	6.8	14.4	3.3	12	15.3
Pow. cons. (mW)	84	18	25.2	15	11.2

V. CONCLUSION

A 3−8 GHz two stages CMOS power amplifier aiming for 1~3 Group of MB-OFDM UWB applications is demonstrated in this paper. The PA is designed and simulated in 0.13μm UMC CMOS technology. The cascade and cascode topology have been used to obtain high gain and low power consumption. Shunt feedback is used to enhance bandwidth and improve wide matching. Simulation results show that proposed design has significantly increase gain and PAE while consuming only 11.2 mW.

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