Linearization of harmonic controlled three-stage Doherty amplifier

Aleksandar Atanasković, Nataša Maleš-Ilić and Bratislav Milovanović

Abstract — In this paper the operation behavior of three-stage Doherty amplifier loaded with harmonic control circuits is analyzed, including the efficiency and linearity. Amplifier is designed in configuration with two quarter-wave impedance transformers in the output combining circuit with LDMOSFETs in carrier and peaking amplifies with the same periphery. The signals for linearization: the fundamental signals' second harmonics-IM2 and fourth-order nonlinear signals-IM4 are extracted at the output of peaking cells, injected at the input and output of the carrier cell suppressing the third- and fifth order intermodulation products of Doherty amplifier.

***Keywords* — Doherty amplifier, harmonic control circuit, fourth-order nonlinear signals, linearization, power-added-efficiency, second harmonics.**

I. Introduction

MORE than ever, the modern wireless communication industry has increased interest for the high-efficient and linear amplifiers to accommodate current communication standards. The third generation (3G) and beyond communication standards offer high data rate transmission and transmit power that carries high-peak-to-average ratio signals. Therefore, base-station amplifiers operate most of their time at lower power level than their maximum, which consequently degrades the efficiency. The Doherty amplifier, which is capable of achieving the requirements of the power amplifiers in base station concerning high efficiency, becomes attractive for wireless industry. The linearity of high power Doherty amplifier was improved using "post-distortion-compensation" [1], the feedforward linearization technique [2], the predistortion linearization technique [3] and combination of those two linearization techniques [4].

The linearization effects of the fundamental signals' second harmonics (IM2) and fourth-order nonlinear signals (IM4) at frequencies that are close to the second harmonics to the standard (two-way, three-way and three-stage) Doherty amplifiers were investigated in [5] by applying the approach where IM2 and IM4 signals are injected together with the fundamental signals into the carrier amplifier input and put at its output [6].

In papers [7] and [8] standard two-way Doherty amplifier was extended to support class-F operation in order to achieve higher efficiency. Additionally, feedforward and digital feedback predistortion linearization technique were implemented in [7] and [8], respectively, to improve the linearity.

The linearity and efficiency of three-stage Doherty amplifier loaded by the diplexers with harmonic control circuit (HCC), which separate fundamental signals and signals for linearization have been analysed [9], [10]. The loading of the carrier and peaking cells, together with the matching circuits at signals for linearization, provides an optimal impedance for their adequate power level and either open circuit for the third harmonics (HCC class-3F) or short circuit for the third harmonics (HCC class-3IF) [9]. Linearization is carried out by the approach that uses IM2 and IM4 signals. Also, the efficiency and linearity of three-stage Doherty amplifier with HCC loading for adequate power of the signals for linearization, which, additionally, represents the open circuit for the third harmonics at the carrier cell output and short circuit at the peaking amplifier outputs (HCC class F-2IF) has been considered [10].

In this paper three-way Doherty amplifier named HCC class-IF-2F is analysed with the combination of the cells loaded with HCC that is the short circuit for the third harmonics at the carrier cell output and open circuit at the two peaking amplifier outputs. The signals for linearization are extracted at output of the peaking cells in Doherty amplifier that are biased at various points to provide the appropriate power levels and phase relations of IM2 and IM4 signals. After been adjusted in amplitude and phase the signals from the output of one peaking amplifier are injected at the input of carrier amplifier while ones appeared at the output of another peaking cell are put to the carrier amplifier output.

Section II includes the design of three-stage Doherty amplifier with harmonic control circuit and circuit for linearization. All results referring to the intermodulation products and efficiency obtained in simulation for two sinusoidal as well as digitally modulated signals by applying the linearization approach are included in section III. The conclusions are reported in section IV.

II. II. Three-stage Doherty Amplifier

A. Design

The amplifier is designed in configuration with two quarter-wave impedance transformers in the output combining circuit [11], [12] as shown in Fig. 1. The carrier and peaking amplifying cells are designed using Freescale's MRF281SR1 LDMOSFET with a 4-W peak envelope power level (PEP) according to the non-linear MET model included in ADS library.

Aleksandar Atanaskovic, Natasa Males-Ilic, and Bratislav Milovanovic are with the Faculty of Electronic Engineering, Aleksandra Medvedeva 14, 18000 Nis, Serbia, (phone:+38118529137 e-mail: aleksandar.atanaskovic; natasa.males.ilic; bratislav.milovanovic @elfak.ni.ac.rs)

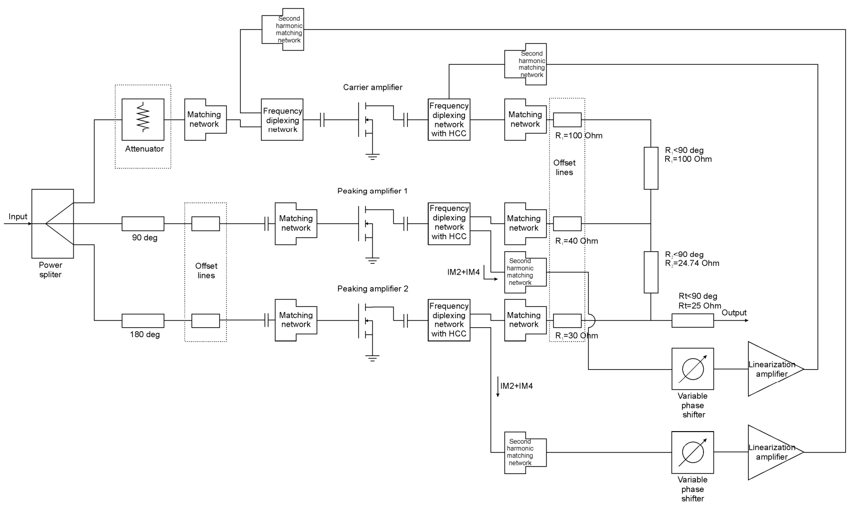


Fig. 1. Three-stage Doherty amplifier with additional circuit for linearization

Doherty amplifying cells are loaded with the frequency diplexer at the outputs that separates the fundamental signals and signals for linearization. The diplexer includes harmonic control circuit (HCC) [9] that, together with the matching circuit, provides the optimal impedance for the signals for linearization. Additionally, it represents the short circuit for the third harmonics at the carrier cell output and open circuit at the peaking amplifier outputs. Doherty amplifier in this configuration is denoted as HCC class-IF-2F.

The matching impedances for source and load of amplifying cells at 2.14GHz are selected to satisfy the high efficiency. The input matching is performed for 50Ω, while the output matching is designed to transform the optimum output impedance of the carrier and two peaking cells to 100Ω, 40Ω and 30Ω, respectively.

The carrier cell is biased at class-AB with $V_G = 5.1\text{V}$ (13.5%I_{DSS}). Two peaking amplifiers operate in class-C. The drain bias voltage $V_D = 26\text{V}$ is the same for all cells.

Offset lines are incorporated at the output of peaking amplifier cells to minimize the effective loading of the peaking amplifiers in state when those amplifiers do not operate (low-power range). In order to compensate for phase relation distortion in Doherty amplifier an appropriated offset line is adjusted at the output of the carrier amplifier.

The peaking amplifiers are driven by signals with 1dB higher power than that of the carrier amplifier according to the analysis of uneven power drive performed in [13]. Maximum output power achieved by the Doherty configuration is 41dBm.

B. Linearization

Theoretical analysis of the linearization approach that uses second harmonics and fourth-order nonlinear signals (IM2 and IM4) for linearization has been given in [5], [6], [9]. According to this, it is possible to reduce spectral regrowth caused by the third- and fifth-order distortion of fundamental signal by choosing the appropriate amplitude and phase of IM2 and IM4 signals injected at the input and output of the amplifier.

The IM2 and IM4 signals generated at the output of peaking amplifiers are extracted through HCC diplexer circuits. It separates the fundamental signals and the signals for linearization (IM2 and IM4 signals) that are matched to the impedance for their adequate power level. Additionally, for the third harmonics HCC provides a short circuit at the carrier cell and an open circuit at the peaking cells. Also, the frequency diplexer in configuration depicted in [5] is inserted at the carrier amplifier input with the independent matching circuits for the fundamental and signals for linearization. Therefore, the linearization of Doherty amplifier is carried out by the simultaneous injection of the IM2 and IM4 signals at the input and output of the carrier amplifier. Those signals are generated at the output of peaking amplifiers that are biased at different points to produce adequate amplitude and phase relations between IM2 and IM4 signals. The IM2 and IM4 signals are tuned in amplitude and phase by the amplifier and phase shifter over two paths as given in Fig. 1.

Consequently, the carrier amplifier is harmonically controlled at input and output. This configuration enables higher gain of class-AB carrier amplifier with lower power of intermodulation products in reference to the standard class-F or class-IF amplifier biased at pinch-off [14].

III. Results

The results that relate to HCC class-IF-2F analyzed herein are compared to HCC class-3IF and class-F-2IF. The analysis includes the optimization of offset line length in the carrier cell output in order to compensate for the time delay between amplifying branches by considering the influence of additional circuit for linearization. The HCC class-3IF and class-F-2IF have been already analyzed in [9] and [11], respectively. However, the length of offset lines was not optimized with the addition of linearization circuits.

The linearization results for two-tone test at frequencies 2.139GHz and 2.141GHz achieved for all designed three-stage Doherty configurations are given in Table 1. It compares output spectra before and after the linearization in case of 20dBm input power of each fundamental signal. It can be noticed that in case of HCC class-3IF Doherty amplifier IM3 products decrease for 19dB and IM5 products go down for 4.5dB and 8dB. When HCC class-F-2IF is considered it is seen that IM3 products appear to be 16dB lower whereas IM5 products are lessened by 9dB and 14dB. In case of HCC class-IF-2F Doherty, IM3 products descent for 24dB and 19dB while IM5 products are lower for 14dB and 21dB. There is no significant degradation of the output fundamental signals in all cases.

TABLE 1. OUTPUT SPECTRUM OF THREE-STAGE DOHERTY AMPLIFIER BEFORE AND AFTER THE LINEARIZATION FOR HCC CLASS-3IF, HCC CLASS-F-2IF AND HCC CLASS-IF-2IF FOR TWO-TONE TEST AT FREQUENCIES 2.139GHZ AND 2.141GHZ

Type	IM3 (dBm)			IM5 (dBm)		
HCC class	Freq. (GHz)	Bef.	Aft.	Freq. (GHz)	Bef.	Aft.
3IF	2.137 2.143	15.22 15.41	-4.12 -4.41	2.135 2.145	4.21 6.07	-0.32 -2.24
F-2IF	2.137 2.143	16.17 16.40	-0.10 -0.40	2.135 2.145	3.78 6.51	-4.49 -7.06
IF-2F	2.137 2.143	16.14 16.06	-8.08 -3.36	2.135 2.145	5.22 6.40	-8.96 -14.98

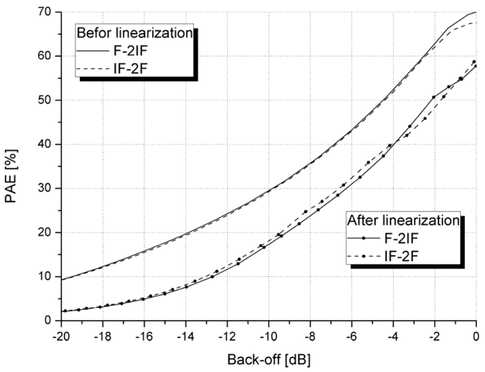
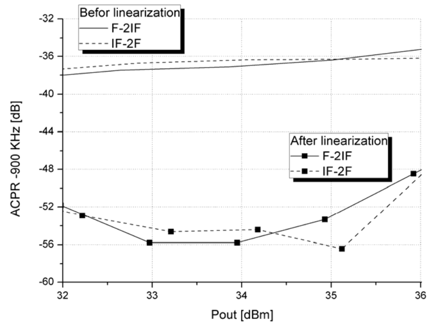


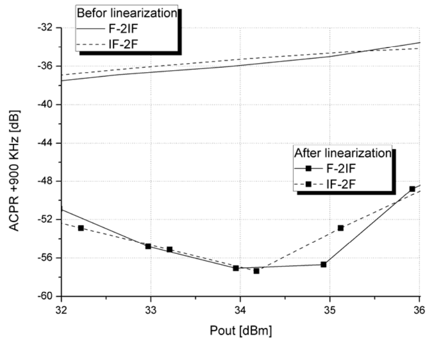
Fig. 2. Power-added-efficiency of three-stage Doherty amplifier

Power-added-efficiency for three-stage Doherty amplifier designed with HCC load for class-IF-2F and class-F-2IF operation is presented in Fig. 2. PAE before linearization relates to the case when amplifying cells are loaded for operation at standard class-F (short circuit for the second harmonics and open circuit for the third harmonics) or IF (open circuit for the second harmonics and short circuit for the third harmonics) in combinations denoted as class-F-2IF and IF-2F. A quiescent bias of carrier cell is 3.8V (pinch-off), a standard bias point for class-F and IF operation. Fig. 2 shows that PAE in case of the additional linearization circuit (carrier cell is now biased at 5.1V) drops in reference to the case of Doherty without linearization, so that it is 59% and 58% at maximum power (0dB back-off) and 33% and 31% at 6dB back-off (35dBm total output power) for HCC class-IF-2F and class-F-2IF, respectively. Therefore, it can be seen almost the same behaviour of PAE characteristic in both combinations of HCC loading circuits.

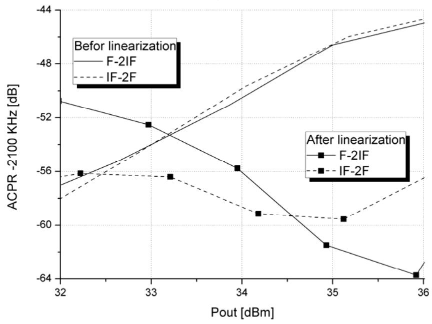
The results from Fig. 3 show the effects of three-stage Doherty amplifier linearization for HCC class-IF-2F and class-F-2IF in case of CDMA digitally modulated signal with 1.25MHz spectrum width, carrier at frequency 2.14GHz. The figures relate to the improvement of adjacent channel power ratio (ACPR) at ±900kHz and ±2100kHz offsets from carrier frequency accomplished for the average output power ranging from 32dBm to 36dBm. The presented results relate to the case when the amplitudes and phases of IM2 and IM4 signals are adjusted on the optimal values for 35dBm average output power.



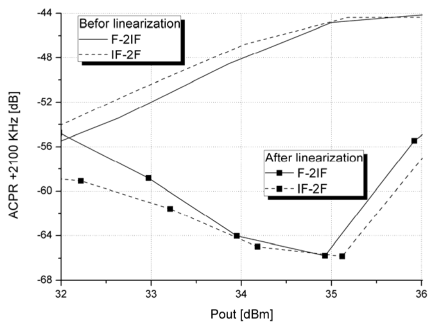
a)



b)



c)



d)

Fig. 3. ACPR before and after linearization in case of HCC class-F-2IF and class-IF-2F three-stage Doherty amplifier for a power range at offsets from carrier frequency: a) -900kHz; b)+900kHz; c) -2100kHz; and d) +2100kHz

It is evident from the Fig. 3 that the linearization with the proposed approach gives satisfactory results in reduction of IM3 products in the entire range of output power for both configurations. When IM5 products are considered, slightly more balanced suppression was achieved for class-IF-2F.

TABLE 2. ACPR AT OFFSETS ±900KHZ AND ±2100KHZ FROM CARRIER FREQUENCY FOR THREE-STAGE DOHERTY AMPLIFIER BEFORE AND AFTER THE LINEARIZATION FOR HCC CLASS-3IF, HCC CLASS-F-2IF AND HCC CLASS-IF-2F IN CASE OF CDMA DIGITALLY MODULATED SIGNAL

Type	ACPR (dB)			ACPR (dB)		
HCC class	Offset (MHz)	Bef.	Aft.	Offset (MHz)	Bef.	Aft.
3IF	-0.9 +0.9	-37.90 -36.38	-48.88 -52.11	-2.1 +2.1	-46.78 -45.92	-66.23 -67.61
F-2IF	-0.9 +0.9	-36.40 -35.00	-53.34 -56.68	-2.1 +2.1	-46.29 -44.82	-61.48 -65.78
IF-2F	-0.9 +0.9	-36.31 -34.52	-56.43 -52.88	-2.1 +2.1	-45.95 -44.37	-59.54 -65.82

The ACPRs obtained in simulation before and after the linearization for CDMA digitally modulated signal with input power 23dBm are compared in Table 2 for all combinations considered. ACPR is improved for approximately 11dB and 16dB at ±900kHz and 19dB at ±2100kHz for HCC class-3IF. In case of HCC class-F-2IF the improvement is around 17dB and 22dB at ±900kHz and 15dB and 21dB at ±2100kHz. ACPR gained for class-IF-2F Doherty amplifier are almost the same: 20dB and 18dB at ±900kHz offsets and 14dB and 21dB at ±2100kHz offsets.

Additionally, the output spectra obtained in simulation before and after linearization for HCC class-IF-2F, with output power 35dBm are shown in Fig. 4.

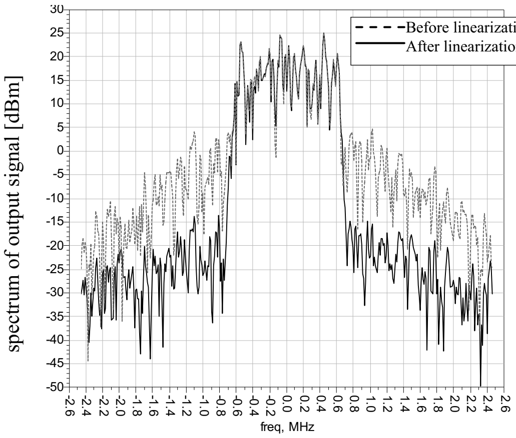


Fig. 4. Simulated spectrum of the output signal for HCC three-stage Doherty amplifier for CDMA digitally modulated signal

IV. CONCLUSION

This paper presents the design of three-stage Doherty amplifier with LDMOSFETs in carrier and peaking amplifies loaded with the frequency diplexer at the outputs. It includes a harmonic control circuit that, together with the matching circuits, enables an optimal impedance for adequate power of the signals for linearization as well as a short circuit for the third harmonics at the output of the carrier cell and an open circuit at the output of peaking cells. For this configuration of three-stage Doherty amplifier (denoted as HCC class-IF-2F) the linearization is carried out with the simultaneous injection of the second harmonics and fourth-order nonlinear signals (IM2 and IM4) at the input and output of the carrier cell. The linearization approach achieves very good results in the reduction of both IM3 and IM5 products retaining the high efficiency of Doherty amplifier (33% at 6dB back-off point). Moreover, since the peaking amplifiers are exploited as sources of signals for Doherty amplifier linearization there is no need for the additional nonlinear sources, which leads to lower energy consumption and simpler linearization circuit topology.

ACKNOWLEDGMENT

Authors would like to thank Ministry of Science and Technological Development of Republic of Serbia for supporting the research reported in this paper.

REFERENCES

[1] K. J. Chao, W. J. Kim, J. H. Kim and S. P. Stapleton, “Linearity Optimization of a High Power Doherty Amplifier based on Post-Distortion Compensation”, *IEEE Microwave and Wireless Components Letters*, vol.15, no.11, pp.748-750, 2005.

[2] K. J. Cho, J. H. Kim and S. P. Stapleton, “A Highly Efficient Doherty Feedforward Linear Power Amplifier for W-CDMA Base-Station Applications”, *IEEE Trans., Microwave Theory Tech.*, vol. 53, no. 1, pp.292-300, 2005.

[3] B. Shin, J. Cha, J. Kim, Y. Y. Woo, J. Yi, B. Kim , “Linear Power Amplifier based on 3-Way Doherty Amplifier with Predistorter”, *IEEE MTT-S Int. Microw. Symp. Digest*, pp.2027-2030, 2004.

[4] T. Ogawa, T, Iwasaki, H. Maruyama, K. Horiguchy, M. Nakayama, Y. Ikeda and H. Kurebayashi, “High efficiency feed-forward amplifier using RF predistortion linearizer and the modified Doherty amplifier”, *IEEE MTT-S Int. Microw. Symp. Digest*, pp.537-540, 2004.

[5] Aleksandar Atanasković, Nataša Maleš-Ilić, Bratislav Milovanović, “The Linearization of Doherty Amplifier”, Microwave review, No.1, Vol. 14, pp.25-34, September 2008.

[6] A. Atanasković, N. Maleš-Ilić, B. Milovanović, “The Suppression of Intermodulation Products in Multichannel Amplifiers Close to Saturation”, *Proceedings of 11th WSEAS International Conference on Circuits*, pp. 198-201, Greece, July 2007.

[7] Y. Suzuki, T. Hirota and T. Nojima, “Highly Efficient Feed-Forward Amplifier using a class-F Doherty Amplifier“, *IEEE MTT-S Int. Microw. Symp. Digest*, pp.77-80, 2003.

[8] J. Kim, J. Moon, Y. Y. Woo, S. Hong, I. Kim,J. Kim and B. Kim, “Analysis of a Fully Matched Saturated Doherty Amplifier with Excellent Efficiency“, *IEEE Trans. Microwave Theory and Techniques,* vol. 56, pp. 328-339, 2008.

[9] Nataša Maleš-Ilić, Aleksandar Atanasković, Bratislav Milovanović: “Harmonic-Controlled Three-stage Doherty Amplifier with Improved Linearity”, *WSEAS Transaction on Circuits and Systems*, WSEAS Press, Vol.8, Issue 9, pp.769-778, September 2009, ISSN:1109-2734

[10] Nataša Maleš-Ilić, Aleksandar Atanasković, Bratislav Milovanović: “Linearization of Harmonic Controlled Three-stage Doherty Amplifier“, *Elektronski zbornik radova 53 konferencije ETRAN 2009 na CD-u*, Vrnjačka Banja, Srbija, 15-18. Jun, Društvo za ETRAN, MT2.3, 2009, ISBN:978-86-80509-64-8.

[11] N.Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, “Analasys and Design of a High-Efficiency Multistage Doherty Power Amplifier for Wireless Communicaton”, *IEEE Trans., Microwave Theory Tech.*, vol. 53, no. 3, pp. 852-860, 2005.

[12] M. J. Pelk, W. C. E. Neo, J. R. Gajadharsing, R. S. Pengelly, and L. C. N. de Vreede, ”A High-Efficiency 100-W GaN Three-stage Doherty Amplifier for Base-Station Applications”, *IEEE Trans., Microwave Theory Tech.*, vol. 56, no. 7, pp. 1582-1591, 2008.

[13] J. Kim, J. Cha, I. Kim, and B. Kim, “Optimum Operation of Asymmetrical-Cells-Based Linear Doherty Power Amplifiers-Uneven Power Drive and Power Matching“, *IEEE Trans., Microwave Theory Tech.*, vol. 53, no. 5, pp. 1802-1809, 2005.

[14] B. Ingruber, M. Wachutka, “High-Efficiency Harmonic-Control Amplifier”, *IEEE Trans. Microwave Theory and Techniques,* vol. 46, pp. 857-862, 1998.