

A CMOS Energy-Detector for Impulse-Radio UWB Noncoherent Receivers

Ganga Bahubalindrani, Cândido Duarte, *Student Member, IEEE*, Daniel Oliveira, *Student Member, IEEE*, Vítor Grade Tavares, *Member, IEEE*, and Mirjana Videnovic-Misic *Member, IEEE*

Abstract—This paper presents the design of an energy detector for ultra-wideband impulse-based applications. It comprises a squarer using a passive mixer and an integrate-and-dump circuit on a single stage. A current-reuse topology was chosen to reduce the overall power consumption. The proposed energy detector targets low data-rate communications for noncoherent receivers, using on-off keying modulations. The circuit has been designed in a CMOS 180-nm process with 1.8-V power supply. The simulation results show a total power dissipation of 287- μ W for a 1-Mbps data-rate using an indoor channel model.

Index Terms—impulse-radio ultra-wideband, analog squarer, integrate-and-dump, noncoherent receiver.

I. INTRODUCTION

IMPULSE-RADIO ultra-wideband (IR-UWB) has recently become one of the most inspiring technologies for a great diversity of emerging wireless applications. IR-UWB relies on the transmission of sub-nanosecond pulses with reduced amplitudes. Due to the broadband spectrum of short-pulse waveforms, the susceptibility against multipath fading is strongly reduced, which fits common requirements of most modern indoor short-range applications [1]. Moreover, IR-UWB interfaces allow the implementation of low-cost/low-power solutions well-suited to the typical purposes of some emerging applications, such as wireless sensor networks [2] and biomedical implants [3].

The detection of narrow pulses with power levels close to the noise floor poses challenging specifications in IR-UWB receiver designs. Noncoherent detection provides energy-efficient demodulation for data rates in the range of 1-kbps up to several Mbps [4]–[6]. Pulse synchronization can be greatly relaxed when compared to complex schemes based on coherent demodulation. Although the noncoherent demodulation is more sensitive to channel noise, it is attractive due to low-power consumption, simplicity and low-cost implementation.

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G. Bahubalindrani, C. Duarte, D. Oliveira and V. G. Tavares are with INESC Porto, Portugal, and also with FEUP – Faculty of Engineering, University of Porto, Rua Dr. Roberto Frias, s/n, 4200-465 Porto, Portugal (e-mail: vgt@fe.up.pt).

M. Videnovic-Misic is with the Department of Power, Electronics and Communications Engineering, Faculty of Technical Sciences, University of Novi Sad, Trg Dositeja Obradovića 6, 21000 Novi Sad, Serbia (phone: 381-21-485-2055; e-mail: mirjam@uns.ac.rs)

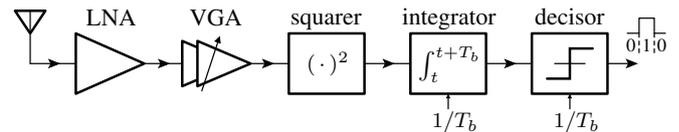


Fig. 1. IR-UWB noncoherent receiver.

Fig. 1 shows the block diagram of a noncoherent IR-UWB receiver. The system explores the reduced complexity of on-off keying detection (OOK) suitable for low data-rates. An incoming signal is firstly amplified by a wideband low-noise amplifier (LNA), which is followed by a variable-gain amplifier (VGA) chain. The UWB signal is then applied to an energy detector, which comprises a self-mixer and an integrator. The energy estimation of an incoming bit is obtained from the resulting UWB squared signal integration along the bit time-frame. A comparator then discriminates the received energy-level from the noise floor produced in the absence of pulses.

This paper presents a CMOS design for an energy detector of an IR-UWB receiver. The proposed circuit mainly targets low-power consumption both on the squarer and integrator. The remainder of this paper is as follows. Section II presents an overview of energy detectors based on squaring circuits. Section III describes the proposed circuit topology for the energy detector and the following section reports simulation results. Finally, in Section V concluding remarks are given.

II. ENERGY DETECTORS OVERVIEW

Energy detection is a low-complexity method appropriate for OOK demodulation. The basic structure of an energy detector includes a squarer followed by an integrator and a comparator, as shown in Fig. 1. The squarer stage estimates the instantaneous power of an incoming signal. The high-frequency components resulting from the product are then filtered at the integrator, while the average power is simultaneously computed during a time period of a bit.

Most squaring circuits reported in literature use a self-mixer architecture (i.e. a mixer with shorted inputs) to obtain the squared signal. In [6], the authors employ a Gilbert-based topology to perform the squaring operation. Alternatively, the authors in [5] use gate and source injection to obtain a squared gate voltage. Both topologies can provide positive dB conversion-gain, but at the cost of relatively high-power dissipation and die area. In [7] it is presented an ultra low-power squarer based on a differential amplifier as source follower. The proposed solution has a simple structure, nevertheless it is prone to dc-offset variations that can corrupt the base-band

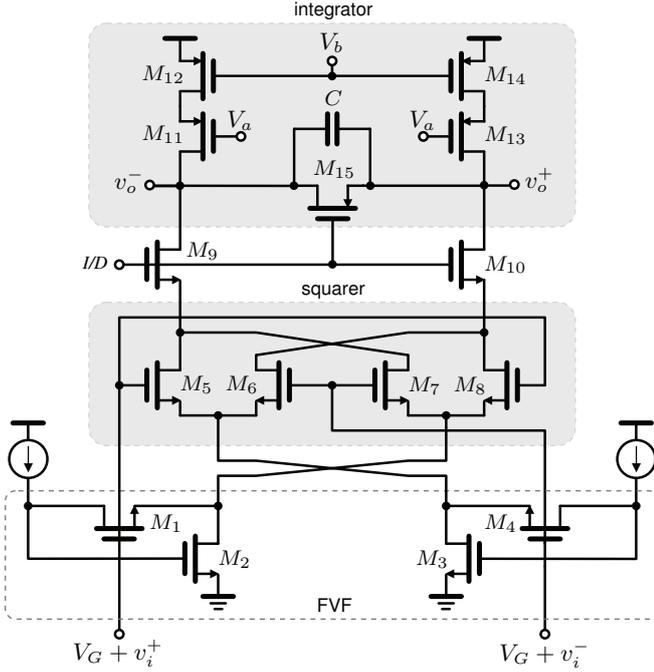


Fig. 2. Proposed IR-UWB energy detector.

signal. The squarer proposed in [8] is based on the MOS square-law in saturation region. It uses a replica circuit with ac grounded-inputs so that offset-voltage cancellation can be achieved at the output.

Passive mixers are also an interesting alternative, at least from the low-power perspective [9]. A passive mixer is proposed in [4] for an IR-UWB noncoherent receiver. However, no detail is given on the actual implementation of the circuit, particularly on how the squarer drives the integrator. In [10], the authors propose a simple squarer topology with MOSFETs operating in triode region. The squarer is followed by a current amplifier that drives an integrator.

In this paper we present the design of a CMOS energy detector that incorporates a passive mixer and integrator within the same stage. The design approach targets overall low-power consumption.

III. PROPOSED CIRCUIT

The proposed energy detector is shown in Fig. 2. The transistors M_5 – M_8 form the passive mixer, i.e. the squarer. Since two of the squarer inputs are source terminals of NMOS devices, voltage buffers are required to prevent gain losses in upstream amplifier stages. A flipped voltage follower (FVF) configuration [11] presents satisfactory bandwidth for IR-UWB applications [12], being a natural choice for voltage buffering. Transistors M_1 – M_4 constitute two buffers based on the FVF configuration.

The existence of capacitors in the signal path has quite impact on the circuit transient response. In order to minimize the system turn-on time, a dc coupling is preferred between the squarer inputs and the voltage buffer. Nonetheless, at some point this approach also limits the circuit performance since there is less design freedom for transistor sizing.

Transistors M_9 and M_{10} impose a fixed voltage at the squarer output. The voltage signal I/D controls the integration time of the squared current and defines M_9 – M_{10} operation modes, either cut-off or biased in strong inversion. At the end of an integration period, the control signal I/D drops to zero cutting M_9 and M_{10} . Since no current can flow (except in the FVF buffer) the squarer circuit goes into idle mode, avoiding static current consumption.

The integrate-and-dump circuit is stacked on top of the squarer. By reusing the same bias current, the overall power consumption is lowered. The cascode transistors M_{11} – M_{14} act as active loads that maximize the output impedance. During the time interval of a bit, the differential current drawn from the squarer is integrated in the capacitor connected between the output nodes. At the end of the integration window, signal I/D sets the squarer to idle mode and voltage dumping takes place. At that time, the PMOS transistor M_{15} is activated and C is fully discharged so that new pulses can be processed.

A. Passive Squarer

Fig. 3 shows the simplified circuit of the proposed squarer. A constant voltage V_D is assumed at the drains of the transistors (set by M_9 – M_{10} during the integration period).

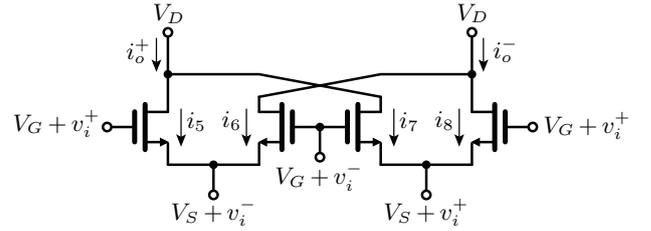


Fig. 3. Circuit used on the analysis of the squarer.

Referring to the notation depicted in Fig. 3 and assuming all the transistors operating in the triode region, $V_D < V_G - V_t$ and $V_G - V_S > V_t$ where V_t is the threshold voltage, one can write the drain currents as follows

$$i_o^+ = i_5 + i_7 = I_\alpha + \frac{1}{2} \cdot \beta \cdot [(v_i^+)^2 + (v_i^-)^2 - 4v_i^+ v_i^-] \quad (1)$$

$$i_o^- = i_6 + i_8 = I_\alpha - \frac{1}{2} \cdot \beta \cdot [(v_i^+)^2 + (v_i^-)^2] \quad (2)$$

where β is the transconductance parameter assuming equal sized transistors. The term I_α is the resulting common-mode drain current given by

$$I_\alpha = \beta [(v_i^+ + v_i^-)(V_D - V_G + V_t) - V_D^2 + V_S^2 + 2(V_G - V_t)(V_D - V_S)] \quad (3)$$

The squared signal can be obtained from the differential currents at the drain

$$i_o = i_o^+ - i_o^- = \beta \cdot (v_i^+ - v_i^-)^2 \quad (4)$$

According to (4) one can make use of differential signals at the input, i.e. $v_i^+ = -v_i^-$, or alternatively connect one input to the ac-ground, performing squaring operation in both cases. When the squarer is driven by a single-ended LNA, the latter avoids the use of a UWB balun [8], which is an energy-expensive solution with a typical power consumption

in the order of mili-watts [13]. The only drawback for the grounded-input approach is that the current gain is reduced to one half. In this work a differential input has been chosen to benefit from the common-mode noise rejection.

B. Integrate-and-Dump

Fig. 4 shows the simplified representation of the integrate-and-dump circuit. The impedance R_o represents the equivalent impedance seen at each output node. Transistors M_9 and M_{10} provide unitary-current buffering (Fig. 2). Assuming $v_i = v_i^+ - v_i^-$, the squarer can be seen as a current source with value given by (4).

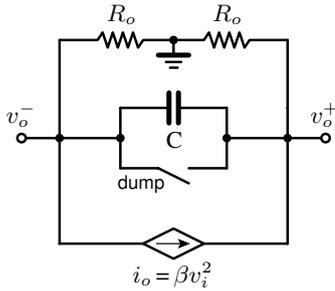


Fig. 4. Simplified equivalent circuit for the integrator.

For a null voltage at the end of dumping, during the integration interval T_i and as long as $R_o \gg T_i/(2C)$, the output voltage is given by

$$v_o = v_o^+ - v_o^- \approx \frac{\beta}{C} \int_{t_0}^{t_0+T_i} v_i^2 dt \quad (5)$$

Pulse repetition per single bit is a common method employed to facilitate the demodulation process [5]. Therefore, the time constant of the integrator needs to be designed in accordance with the integration time T_i considering the pulse repetition rate (PRR). Moreover, the noise level needs also to be properly estimated to define the time constant. Otherwise, the integrator can saturate in the absence of incoming pulses. To accommodate for different PRRs and noise conditions, the capacitor C in the proposed circuit can be further replaced by a digitally-controlled capacitor bank.

IV. SIMULATION RESULTS

The proposed circuit has been designed in a 180-nm RF-CMOS process with 1.8-V power supply. The design has been simulated with Cadence Spectre-RF using BSIM3v3 MOSFET models.

At low data-rates, IR-UWB allows the receiver to be in the idle mode during long periods of time [4], [6]. Low duty-cycle has been used in the proposed demodulation scheme. Fig. 5 shows an input test signal comprising a pulse sequence in which, for each transmitted bit several fifth-order Gaussian pulses are repeated within a data rate of 1-Mbps. The channel has been modeled considering frequency-dependent propagation losses, for residential line-of-sight (LOS) applications from 2 to 10-GHz [14].

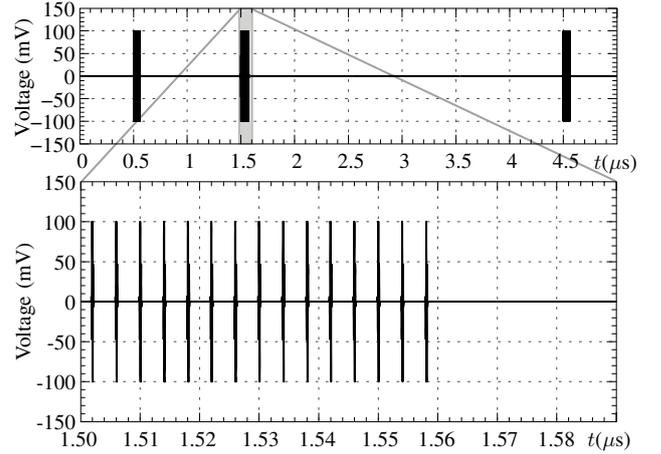


Fig. 5. Voltage waveforms at the differential input of the voltage buffer.

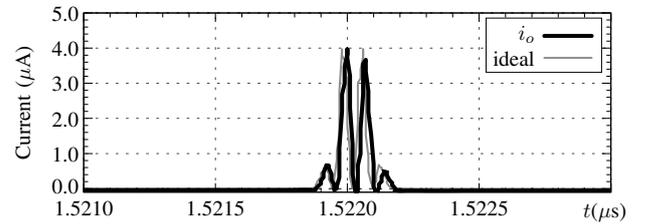


Fig. 6. Current at the squarer and ideal squared-input (normalized).

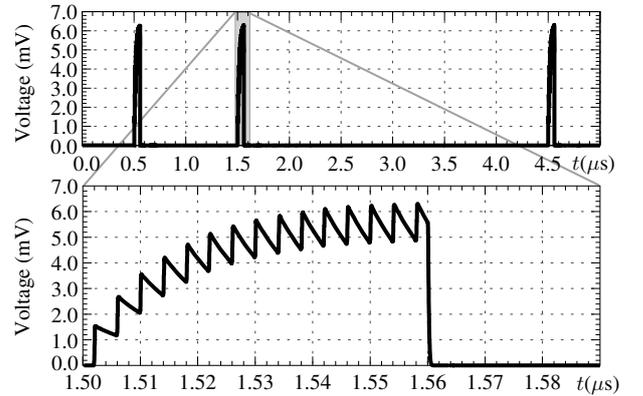


Fig. 7. Differential output of the integrator.

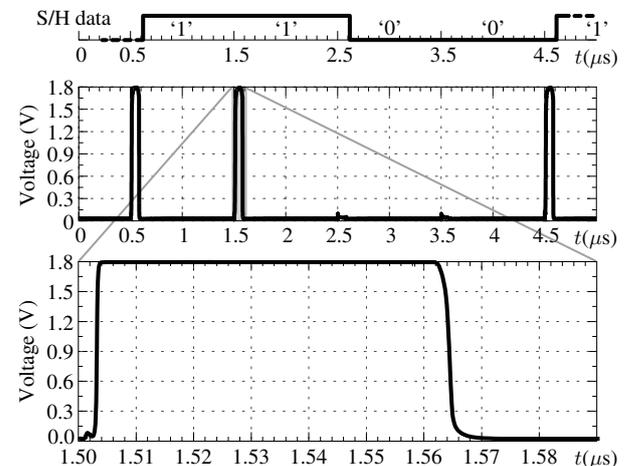


Fig. 8. Output of the comparator.

Fig. 6 shows the square of the UWB pulse and the square of the voltage input, to validate the circuit squaring operation. The integration of the squared signals is plotted in Fig. 7. Reset occurs at the end of the integration interval. The zoomed area of the figure represents an example of an integration interval.

To demonstrate the viability of the proposed topology a high-speed decisor has been also implemented, which includes an amplifier chain and a comparator. Since the passive mixer does not provide high current gain, the voltage at the integrator output is relatively low. A 22-dB gain single stage amplifier has been designed to further increase this voltage. The amplifier is based on an NMOS differential-pair with PMOS cascode loads. As an example of the received bit-sequence '11001', the detector output is shown in Fig. 8. The total power dissipation of the proposed circuit is lower than 600- μ W including the decisor circuits. Nevertheless, the detailed discussion of the decisor topology and its performance is out of the scope of this article and would be addressed in some other paper.

Table I summarizes the performance of the proposed circuit and compares it with other works from literature (simulation results only). The power dissipation for proposed circuit is only 287- μ W. One should note that this includes the voltage buffers, squarer and the integrator, while in the other cases the power consumption is relative solely to the squarer. This demonstrates high power efficiency of the proposed topology.

TABLE I
POWER CONSUMPTION OF IR-UWB SQUARERS

Ref.	Squarer	Process
[7]	86.5- μ W	180-nm
[12]	10.8-mW	180-nm
[15]	52-mW	180-nm
[16]	1.7-mW	180-nm
[17]	720- μ W	65-nm
This work	287- μ W	180-nm

V. CONCLUSION

A low-power energy detector was presented in this paper. A single stage squarer and integrator was proposed based on current reuse technique to achieve low-power consumption. The circuit has been tested with a train of impulses including frequency-dependent channel losses modeling. The proposed topology dissipates only 287- μ W. A decision circuit was also implemented in order to prove the feasibility of the squarer-integrator circuit. Results show that the proposed circuit is a good solution for low data-rate UWB applications.

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