An UWB 3–5 GHz Common-Gate Low Noise Amplifier Designed in 0.13µm Technology

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***Abstract* — In this paper design of low noise amplifier (LNA) for the low frequency band, 3–5 GHz, in UMC 0.13µm CMOS technology is presented. In order to achieve good input matching common-gate topology is used. High gain with low power consumption is obtained using cascade circuit configuration. LNA shows less than –10.91 dB input return loss (S_{11}) and less than –11.81 dB output return loss (S_{22}), noise figure (NF) of 3.56 dB to 3.98 dB, maximum gain (S_{21}) of 21.25 dB while dissipating 5.54 mA from 1.2 V supply. The high circuit stability parameters $K_f > 58.83$ and $B_{1f} > 0.98$ are obtained.**

***Keywords* — Common-gate configuration, low noise amplifier (LNA), ultra-wideband (UWB).**

I. Introduction

ULTRA-WIDEBAND (UWB) presents an emerging, low power technology applicable for short-range, high-speed wireless communications. Allocated band (IEEE 802.15.3a) for UWB system is between 3.1–10 GHz [1]. Low frequency band, from 3.1–5 GHz, is used for development of the first generation of UWB systems. Two major solutions: Multi-band Orthogonal Frequency Division Multiplexing (MB-OFDM) [2], based on frequency hopping, and Direct Sequence UWB (DS-UWB) [3] are proposed to transmit the data rate up to 480 Mbps by using only this low frequency band.

Design of low noise amplifier (LNA) maintains to be one of the challenging tasks in up-to-date receiver design. Being the first circuit in the receiver's chain it must meet several stringent requirements. It needs to provide sufficient gain to amplify received weak signal and to overcome the noise of the subsequent stages, adequate input and output matching to improve reflection coefficients and low noise figure (NF) to improve sensitivity. All this have to be fulfilled within defined (wide) bandwidth and with low power consumption.

In this paper two-stage, cascode common-gate in cascade with cascode common-source, broadband LNA topology, is proposed. In Section II basic circuit techniques, given in literature, are described, while chosen topology is analyzed in Section III. Simulated figures of merit (FOMs) are given in Section IV followed by discussion and comparison with other UWB LNA designs found in literature. The Section V concludes the paper.

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II. UWB Design Techniques

Four basic circuit designs are proposed to obtain UWB LNA: distributed amplifier, inductively degenerated common source amplifier incorporated with additional input band-pass LC-filter, common source amplifier with resistive shunt-feedback and common gate circuit.

A. Distributed amplifier

Distributed approach is shown in Fig.1. Parasitic capacitance of the input transistor is absorbed as part of the transmission line, which leads to wide frequency band operation. To achieve necessary gain several amplifying stages are needed. Consequently, this approach is power hungry and area consuming. Moreover, difficult NF optimization for this technique is still an issue [4].

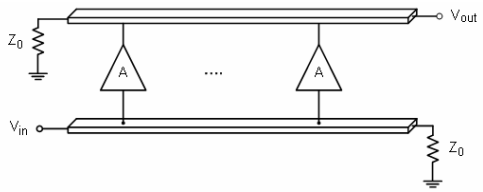

Fig. 1. Distributed LNA.

B. Inductive degenerated common-source amplifier incorporated with input network

The inductively degenerated common source amplifier integrated with additional input band-pass LC-filter, shown in Fig.2, represents another technique for achieving broadband input matching. In addition gain flatness and low power consumption are achieved. However, large number of on-chip reactive elements demand high chip area and degrade NF at higher frequencies [5].

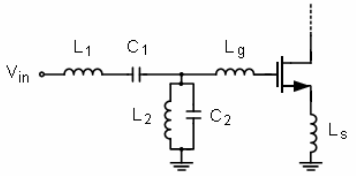

Fig. 2. Common-source LNA with LC input network.

C. Resistive shunt-feedback configuration

In Fig. 3 resistive shunt-feedback is employed with common source amplifier to provide wideband input matching and flat gain [6], [7]. Input resistance is determined by the feedback resistance divided by the voltage gain of the common source amplifier [8]. To obtain 50 Ω input match, few hundred Ohms for feedback resistance is needed, which results in NF degradation. Moreover, due to strong dependence of voltage gain on the amplifying transistor transconductance, the amplifier requires a large amount of current to achieve high gain.

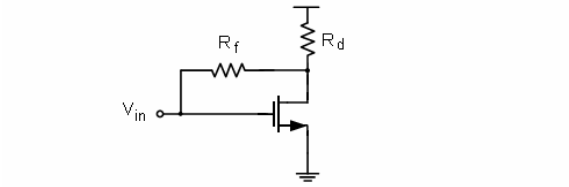

Fig. 3. Common-source LNA with resistive feedback.

III. COMMON-GATE LNA TOPOLOGY

Approach utilizes common-gate circuit, shown in Fig. 4, provides wideband input matching. Main disadvantage of common-gate amplifiers is their relatively low transconductance value that can not provide low noise and high gain in a whole frequency range. This type of amplifier is usually used as the first stage of multi cascade amplifiers where the next stages enhance the amplification bandwidth [9].

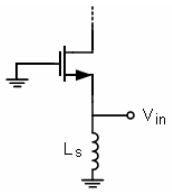

Fig. 4. Common-gate LNA.

The proposed wideband LNA is shown in Fig. 5. It consists of a common-gate stage, a common-source stage and an output buffer.

The common-gate LNA input impedance Z_{in} can be given by:

$$Z_{in} = \frac{j\omega L_s}{1 + (g_{m1} + j\omega C_{gs1}) \cdot j\omega L_s}, \quad (1)$$

where g_{m1} and C_{sg1} is the transconductance and gate-source capacitance of the input RF transistor M_1, respectively. At lower frequency, the input inductor, L_s, provides small impedance to the ground. Hence, Z_{in} is dominated by L_s and the value is almost zero. As frequency increase, g_{m1} become dominant, $g_{m1} >> \omega C_{gs1}$, and the input impedance is defined by $1/g_{m1}$.

Input impedance range is determined by value of L_s. To ensure broad-band input matching condition, optimal value of input inductor, 2.8 nH, is chosen to provide input match close to 50Ω, while low NF, power consumption and high gain are maintained.

Transistors M_1 and M_2, as transistors M_3 and M_4, are connected in cascode to improve the reverse isolation of the circuit. Size of M_1 is designed for proper input matching. Second stage is cascode common-source stage, which provides high gain and determinates higher 3-dB bandwidth of the LNA. Additionally, cascode topology reduces effective M_3 input capacitance and helps to obtain higher gain and broader bandwidth. The source follower, composed of transistors M_5 and M_6, forms the output buffer and provides output wideband matching. All bias circuits are composed of resistors R_{biasn} and R_{refn}, n = 1, 2, 3, and transistor M_n, n = 7, 8, 9, where transistor forms current mirror with corresponding amplifying transistor (M_1, M_3, M_5). To decrease the overall power consumption (P_D), bias transistor width, should be small fraction of amplifying transistor width. The value of R_{biasn} is chosen large enough to provide high impedance path to RF signal while at the same time has small contribution to the circuit noise.

Technique called inductive shunt-peaking, applied by series connection of L_{dn} and load resistance R_{dn}, n = 1, 2, is used to increase bandwidth and improve gain flatness [10].

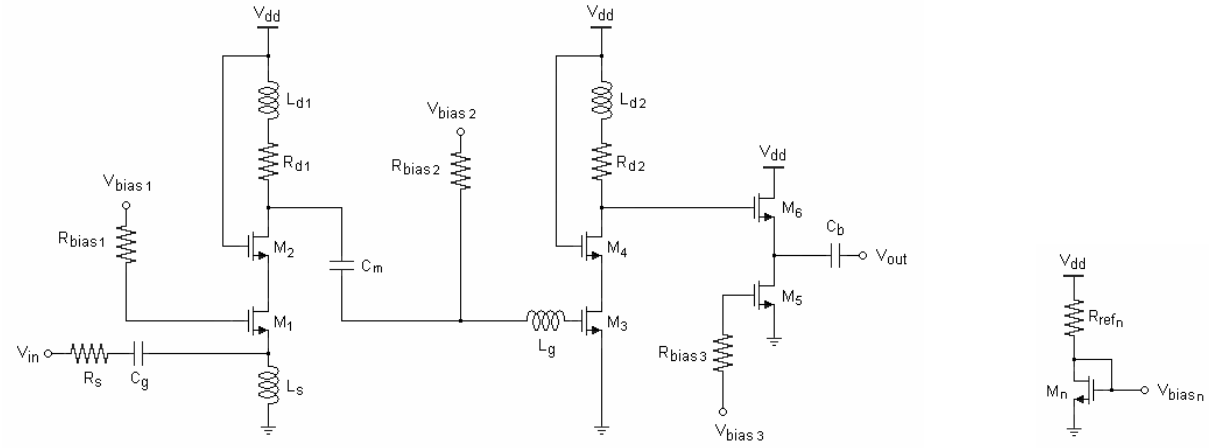

Fig. 5. The designed 3−5 GHz CMOS UWB LNA: (a) amplifying circuit, and (b) biasing circuit.

In addition value of L_{dn} and R_{dn} determines the gain of the first and second stage. Inductor L_g at high frequencies has influence on LNA gain improvement and NF. A coupling capacitor C_m is used to couple RF signal from M_2 to M_3.

Capacitors C_g and C_b are input and output DC blocking capacitors. Their values are chosen large so they do not influence the resonant frequency of the input and output circuit, respectively.

IV. Simulation Results

The designed circuit has been simulated in UMC 0.13µm CMOS eight-metal technology using Spectre Simulator from Cadence Design System. To obtain initial device dimensions and component values the optimization technique with constant power consumption is used [11]. Amplifier was optimized at 4 GHz central frequency. In order to get simulation results as close as possible to measurement results, BSIM3V3 models for all circuit components were introduced. Due to increased complexity of the circuit it was necessary to carefully examine dependence of the LNA FOMs on circuit parameters.

LNA topology was optimized with the main aim to obtain proper input matching, high flat gain, while minimize P_D, NF and keeping acceptable values for remaining FOMs. Simulation results for the common-gate two-stage LNA topology are given in Figs. 6–8 (S_{11} and S_{22}, S_{21}, NF and NF_{min}).

Parameter S_{11} is below –10 dB in the band of interest (–23.57 dB at 3 GHz and –10.91 dB at 5 GHz). This demonstrates the effectiveness of wideband matching realized by common-gate topology. Increase in L_s value results in S_{11} minimum shifted to the lower frequencies, lower NF and higher gain. Further, increasing value of M_1 transistor width will result in lower value of S_{11} minimum, higher S_{21} and lower NF, but power consumption will increase. Change in L_g inductor value influences broadness of S_{11} characteristic. The lowest S_{11} value, –25.74 dB, can be seen at 3.19 GHz. This result is not so close to frequency of 4 GHz for which initial LNA topology was optimized. Shift in frequency value is result of trade-off between proper input matching, high gain and low NF and power consumption, P_D.

Parameter S_{22} is less than –11.81 dB for the whole simulated range. This is achieved by enhancement LNA topology with output buffer. Further excellent reverse isolation (S_{12}) below –60.20 dB is obtained.

Regarding the gain, maximum S_{21} parameter value of 21.25 dB is achieved at 4.05 GHz (18.97 dB at 3 GHz and 18.78 dB at 5 GHz). Variation in S_{21} value in band of interests is 2.5 dB and the 3dB bandwidth covers 2.32 GHz to 5.26 GHz. Cascode common-source transistors values are selected to obtain high gain and broader LNA response, while keeping at the same time P_D at reasonable level.

For voltage supply V_{DD}=1.2 V, a total current including the biasing circuits and output buffer is 5.54 mA. The core consumes 4.45 mA, while the rest is consumed by the buffer (0.67 mA) and biasing circuits (0.42 mA).

NF exhibits a relatively small variation (from 3.56 dB to 3.98 dB) across entire band (3 GHz to 5 GHz). Minimum NF value of 3.56 dB is obtained at 3.88 GHz. This is in accordance with expectations as initial LNA topology is optimized at 4 GHz central frequency. Obtained NF values are close to NF_{min}, the minimum possible NF value.

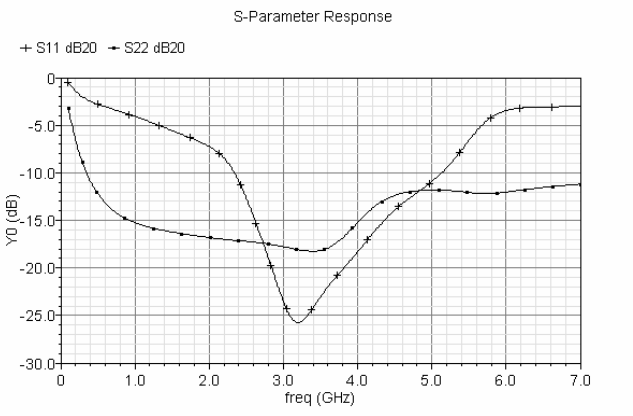

Fig. 6. LNA input (S_{11}) and output (S_{22}) return loss.

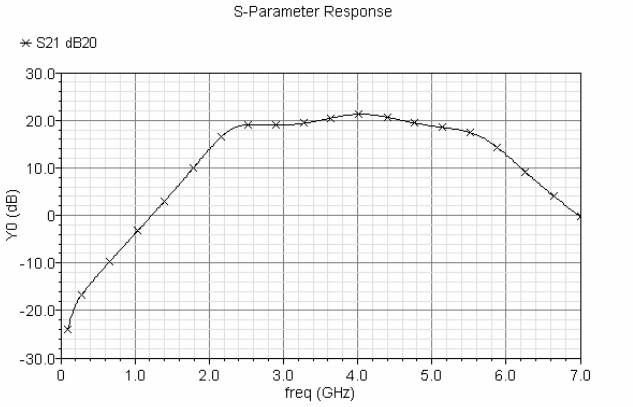

Fig. 7. LNA voltage gain (S_{21}).

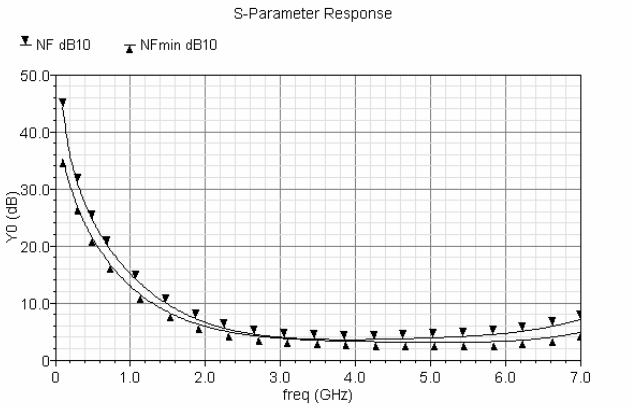

Fig. 8. LNA noise figure (NF) and minimum noise figure (NF_{min}).

Stability parameters simulations were performed from 100 MHz to 7 GHz. Unconditional stability requirements for the whole simulated range is satisfied. Minimum values for stability factors K_f (Rollet stability factor) and B_{1f} (alternate stability factor) are equal to 58.83 and 0.98,

respectively, which are values much higher than 1 and 0 [12], [13].

The optimized FOMs of designed LNA and FOMs values of similar LNA topologies in the frequency band of interest [14], [15], [16] are summarized in Table I. In comparison with LNAs FOMs found in literature, design presented in this paper shows better S_{11} and higher S_{21}. This result is achieved with simple common-gate input stage, without additional improvement techniques such as input filter. While comparing amplifier design in this work and [14], simulated in the same technology, it can be seen that proposed design have better values for input matching. Much higher gain value is achieved by something higher dissipation. Due to aim to obtain high S_{21} and low P_D, resulted in high *NF*. The cascade source degenerated LNA design, presented in [15], achieves good S_{11} value using band-pass filter at a price of large number of reactive elements that causes relatively high power consumption, although low *NF* is achieved. The same gain value is obtained in [16] where current reuse topology is used. The design [16] drawback is high power consumption and higher *NF* since more circuit elements are needed.

TABLE 1: PERFORMANCE COMPARISON OF 3−5 GHZ LNAS.

Ref.	***This work***	***[14]***	***[15]***	***[16]***
S_{11} [dB]	<−10.91	<−10	<−10	<−9
S_{22} [dB]	<−11.81	N/A	<−10	<−8.5
S_{21} [dB]	21.25	11	14	14
NF [dB]	3.98	2.8	2	2.4
P_D [mW]	6.65	5.2	9	12
Technology	0.13µm	0.13µm	0.18µm	0.18µm

V. CONCLUSION

In this paper low-power approach for ultra-wideband low noise amplifier design in the 3–5 GHz band is demonstrated. Using two-stage, cascode common-gate and cascade common-source, topology high gain can be achieved in the desired frequency range consuming only 6.65 mW. Due to the LNA input common-gate stage and output buffer circuit, good input and output matching, respectively, is obtained. This technique gives adequate input match without introducing large number of additionally components (inductors and capacitors). Main disadvantage of this propose in comparison with other designs proposed in literature is higher value of NF. Obtained simulation results prove that matching method used in this paper together with shunt-load peaking is good solution for high gain and low power UWB LNA design.

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